

## WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:  
forming an opening in a dielectric layer  
laser thermal annealing exposed surfaces of the dielectric layer in ammonia (NH<sub>3</sub>)  
and nitrogen (N<sub>2</sub>); and  
5 forming a composite barrier layer comprising tantalum (Ta) lining the opening.
2. The method according to claim 1, wherein the dielectric layer comprises  
fluorine (F) containing silicon oxide derived from F-doped tetraethyl orthosilicate (F-TEOS).
3. The method according to claim 2, comprising laser thermal annealing the  
exposed surfaces to form a surface region depleted in F and enriched in N<sub>2</sub>.
4. The method according to claim 3, comprising forming the composite barrier  
layer by depositing Ta, the composite barrier layer comprising:  
a graded layer of tantalum nitride on the N<sub>2</sub>-enriched surface region, the graded  
tantalum nitride layer containing N<sub>2</sub> in an amount decreasing in a direction away from the N<sub>2</sub>-  
5 enriched surface region; and  
a layer of  $\alpha$ -Ta on the graded tantalum nitride layer.
5. The method according to claim 4, further comprising filling the opening with  
copper (Cu) or a Cu alloy.
6. The method according to claim 5, wherein the opening comprises a dual  
damascene opening having a lower via hole in communication with an upper trench, the  
method comprising filling the opening with Cu or Cu alloy to form a lower via in  
communication with an upper line.
7. The method according to claim 6, comprising laser thermal annealing by  
impinging a laser light beam on the exposed surfaces at a radiant fluence of about 0.09 to  
about 0.11 joules/cm<sup>2</sup>.
8. The method according to claim 7, comprising laser thermal annealing to  
elevate the temperature of about 370°C to about 430°C.

9. The method according to claim 2, comprising laser thermal annealing employing an N<sub>2</sub> flow rate of about 200 to about 2,000 sccm and an NH<sub>3</sub> flow rate of about 200 to about 2,000 sccm to form a region on the exposed surfaces depleted in F and enriched in N<sub>2</sub>.

10. The method according to claim 9, comprising forming the composite barrier layer by depositing Ta, the composite barrier layer comprising:

- a graded layer of tantalum nitride on the N<sub>2</sub>-enriched surface region, the graded tantalum nitride layer containing nitrogen in an amount decreasing in a direction away from the N<sub>2</sub>-enriched surface region; and
- a layer of  $\alpha$ -Ta on the graded tantalum nitride layer.

11. A semiconductor device comprising:

an opening in a dielectric layer; and

a composite barrier layer formed on a surface of the dielectric layer lining the opening; wherein:

- the surface of the dielectric layer comprises a nitrogen (N<sub>2</sub>)-enriched surface region; and
- the composite barrier layer comprises:
  - an initial graded layer of tantalum nitride containing N<sub>2</sub> in an amount decreasing in the direction away from the N<sub>2</sub>-enriched surface region; and
  - a layer of alpha-tantalum ( $\alpha$ -Ta) on the graded tantalum nitride layer.

12. The semiconductor device according to claim 11, wherein the dielectric layer comprises fluorine (F)-containing silicon oxide derived from F-doped tetraethyl orthosilicate (F-TEOS).

13. The semiconductor device according to claim 12, wherein the nitrogen-enriched surface region contains F in an amount less than the remainder of the dielectric layer.

14. The semiconductor device according to claim 13, wherein:

the N<sub>2</sub>-enriched region has a thickness of about 10Å to about 20Å;

the graded tantalum nitride layer has a thickness of about 20Å to about 50Å; and

the  $\alpha$ -Ta layer has a thickness of about 200Å to about 300Å.

15. The semiconductor device according to claim 13, wherein:  
the nitrogen-enriched region contains about 10 to about 40 at.% N<sub>2</sub>; and  
the graded tantalum nitride region contains N<sub>2</sub> in an amount of about 5 to about 15 at.% proximate the N<sub>2</sub>-enriched region decreasing toward the  $\alpha$ -Ta layer.

16. The semiconductor device according to claim 12, wherein the opening is filled with copper (Cu) or a Cu alloy.

17. The semiconductor device according to claim 16, wherein:  
the opening is a dual damascene opening comprising a lower via hole in communication with an upper trench; and  
the filled opening comprises a Cu or Cu alloy via in communication with an upper Cu  
5 or Cu alloy line.

18. The semiconductor device according to claim 11, wherein the dielectric layer comprises a dielectric material having a dielectric constant (k) less than about 3.9.

19. The semiconductor device according to claim 18, wherein the dielectric material is a halogen-containing material.

20. The semiconductor device according to claim 18, wherein the dielectric material is a fluorine (F)-containing oxide.